What is claimed is:

1. A device isolation structure for a semiconductor device, comprising:

a semiconductor substrate in which a field isolation region and an active region are defined, the field isolation region including a plurality of dummy active regions, a plurality of trenches being defined between the dummy active and the active regions; and

a filling layer that fills the plurality of trenches.

2. The structure of claim 1, wherein the filling layer is composed of at least one of a silicon oxidation layer, a boron phosphorous silicate glass (BPSG), a borosilicate glass (BSG), and a phosphosilica glass (PSG).

3. The structure of claim 1, further comprising:

a gate insulation layer positioned on the semiconductor substrate and the filling layer; and

a second conduction layer positioned on the gate insulation layer.

4. The structure of claim 3, further comprising:

a co-salicide layer positioned on the second conduction layer and functioning as a self-aligned silicide layer.

5. The structure of claim 3, wherein the second conduction layer is composed of an undoped polycrystalline silicon.

6. The structure of claim 3, wherein the second conduction layer is a polycrystalline silicon having doped portion corresponding to the active region, the doped layer being doped with an identical impurity.

7. The structure of claim 3, wherein the second conduction layer is a polycrystalline silicon having a doped portion corresponding to the active region, the doped layer being doped with different impurities.

8. The structure of claim 1, wherein the dummy active regions are non-active regions and the active region is an active region.

9. A device isolation structure for a semiconductor device, comprising:

plural dummy active regions positioned adjacent at least one active region within a semiconductor substrate of the semiconductor device; and

a conduction film positioned over the dummy active regions, the conduction film being distinguishable from a gate electrode positioned above the active region of the semiconductor device.

10. The structure of claim 9, further comprising:

a filling layer that fills trenches defined between each of the plural dummy active regions and between the dummy active regions and the active region of the semiconductor device.

11. The structure of claim 9, wherein the conduction film includes undoped polycrystalline silicon.

12. The structure of claim 9, wherein the conduction film includes polycrystalline silicon having a doped portion corresponding to the active region of the semiconductor device, where an impurity used to dope the doped portion is identical to an impurity used to dope the active region of the semiconductor device.

13. The structure of claim 9, wherein the conduction film includes polycrystalline silicon having a doped portion corresponding to the active region of the semiconductor device, where an impurity used to dope the doped portion is different than an impurity used to dope the active region of the semiconductor device.